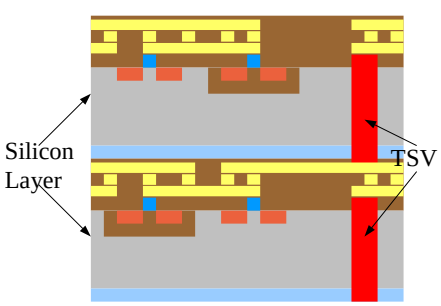
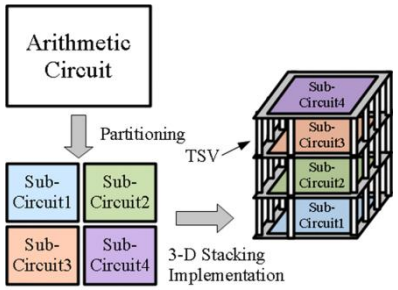
Low-Power High-Performance Computer Architecture

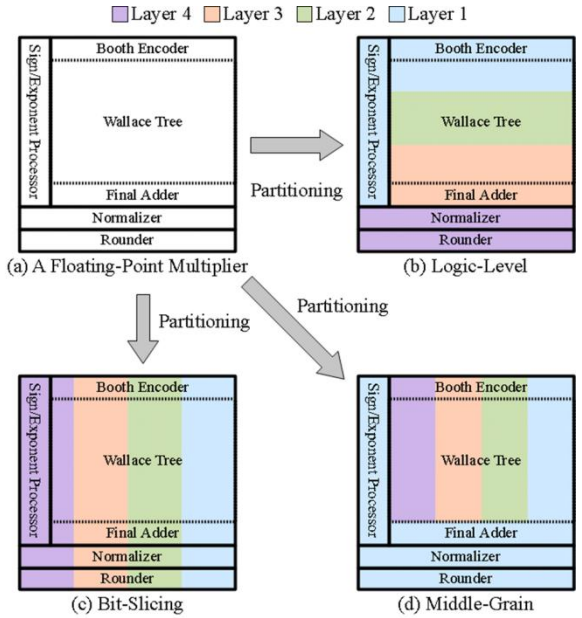
Assistant Professor Jubee Tada



3D-stacked IC technology



3-D implementation of an arithmetic circuit



Partitioning of a floating-point multiplier

Content:

Recently, a 3-D stacked IC technology with through-silicon-via (TSV) is expected to realize low power consumption and high-performance processors.

In the design of 3-D stacked circuits, one circuit is partitioned into several sub-circuits, and each sub-circuit is placed in one layer. This partitioning will affect the performance of 3-D stacked circuits, therefore partition strategies should be discussed to exploit the potential of the 3-D stacked IC technology.

In such a situation, we focus on 3-D stacked arithmetic units and a 3-D stacked cache memory. So far, we have proposed partitioning strategies for 3-D stacked arithmetic units, and designed 3-D stacked arithmetic units based on these strategies.

Yamagata University Graduate School of Science and Engineering
Research Interest : 3D-SIC, Arithmetic Unit, Cache Memory

E-mail : jubee@yz.yamagata-u.ac.jp

Tel : +81-238-26-3576